

# HOMEBREW COMPUTER CLUB

# NEWSLETTER

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Robert Reiling, editor - Post Office Box 626 - Mountain View, CA 94040

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Volume Number 1, Issue 7

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## MAILING ADDRESS

Mail for the club newsletter may be sent to Post Office Box 626, Mountain View, CA 94040. The previous Menlo Park address will be checked for a reasonable time since it has appeared in several publications.

## HARDWARE - Meeting September 17, 1975

The meeting on the 17th was another exciting one with plenty of hardware on display. Included were several Micro-68 units from Electronic Product Associates, Inc., 1157 Vega Street, San Diego, CA 92110. Weatherford is the distributor. This is a neat microprocessor primarily for training, prototype, and system design uses. The SPHERE group took time out from Wescon and demonstrated their equipment at the meeting. Along with their SPHERE 1 computer system they demonstrated a very impressive color graphics display. For more information contact SPHERE Corp., 791 South 500 West, Bountiful, Utah 84010. We received a first look at a system due soon from M&R Enterprises, Post Office Box 1011, Sunnyvale, CA 94088. Perhaps Marty Spergle will give us more details soon. Ken McGinnis had his repackaged ALTAIR set up. He used a Cybercom case very effectively. Another computer system called JOLT was demonstrated by Lynn B. Smith, Microcomputer Associates Inc., 10440 North Tantau Avenue, Cupertino, CA 95014. Lynn put the final touch to the meeting by selecting a name from member address cards turned in during the meeting and giving away a JOLT kit. Dan Wallace was the winner. This kit will be delivered at the next meeting. With activities like those described here you should plan to attend the club meetings and get the latest computer information.

## CLUB POSTER

Scott Spencer suggests a poster that could be put up to spread the word about the club. This is a great idea. Now, we need a poster artist. Who will fill this need? Tell me your ideas.

## BUGBOOK III

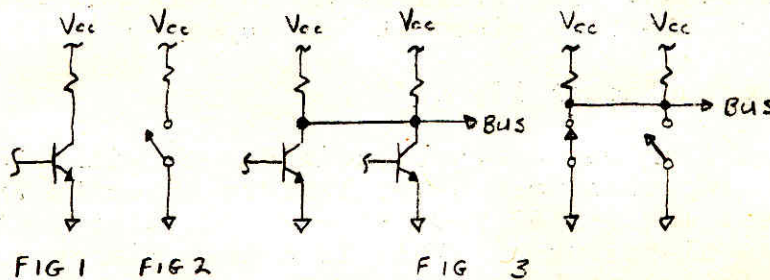
Bugbook III is a new book that has been written to fill the gap between the microcomputer manufacturer's literature and the actual starting point of the potential present day microcomputer users and designers. It has microcomputer interfacing experiments using the Mark 80, an 8080 system, and is published by E and L Instruments, 61 First Street, Derby, Conn. 06418. It is available for \$14.95. The authors Peter R. Rony, David G. Larson, and Jonathan A. Titus have created an excellent book that will delight the experimenter, teacher, and hobbyist.



# TRI-STATE BUSSING - Ray Boaz

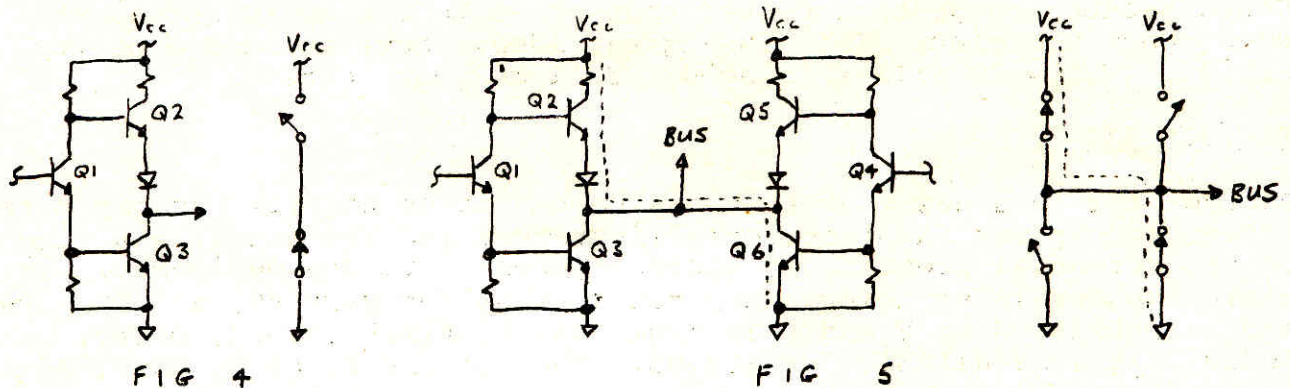
A Tri-State (TSL) gate is the most useful device in any bus-structured system. However, little or no explanation is given as to what a TSL gate is or how it operates. I want to basically talk about the TSL gate in relation to its place in a microprocessor system in terms we all can keep up with. Few systems with more than a limited number of "chips" can do without TSL on their bus lines. Some use open-collector TTL, but this is no replacement for TSL. To appreciate this advance (TSL) in technology we must review the use of diode-transistor logic (DTL) and transistor-transistor logic (TTL) in logic systems of a bus-structured architecture.

The DTL gate output circuit consists of a transistor amplifier and a passive pull-up resistor to  $V_{cc}$  as shown in Fig. 1. This is equivalent to the switch circuit of Fig. 2.



In a bus system the outputs are connected together to form a multisource driver as shown in Fig. 3 (along with its switch equivalent). This type of connection is called a wired-or function, which is really misleading because it does an AND function (all outputs connected must be true for a high level). However, it resulted in a considerable savings of logic and was widely used. A more useful term for "wire-or" connections is collector-dot and will be used here. There is a limit to the number of outputs/inputs (loading) that could be used by collector-dotting due to the paralleling of collector resistors and thus the greater current through the transistor turned on. BUT, it was not a destructive technique. Then along came TTL.

Bussing TTL presented a real problem due to the transistor replacement for the resistor in DTL making a switch or active pull-up to  $V_{cc}$ . The output circuit and its switch equal are shown in Fig. 4. The problem here is that Q1 ALWAYS has either Q2 or Q3 turned on. Therefore, in Fig. 5, if Q1 is on and Q4 is off, there is essentially a short circuit from  $V_{cc}$  to ground as shown by the current path.





This results in the destruction of one or both of the gates. For this reason, standard TTL cannot be used for bussing. Open-collector TTL seemed to be the answer; these gates can be used much like DTL. As a matter of fact, too much like DTL, Fig. 6, shows how we go back almost a generation to "near" DTL operation and over three times slower rates than standard TTL.

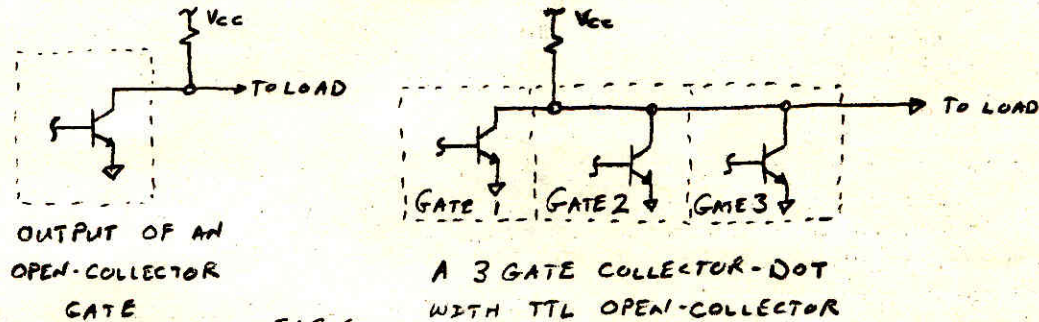


FIG 6

But advance we must--along came TSL.

TSL is the good guy for bussing. Fig. 7 shows the simplified schematic for a TSL gate with its active low, overriding control input. Fig. 7 also shows a standard TTL for comparison.

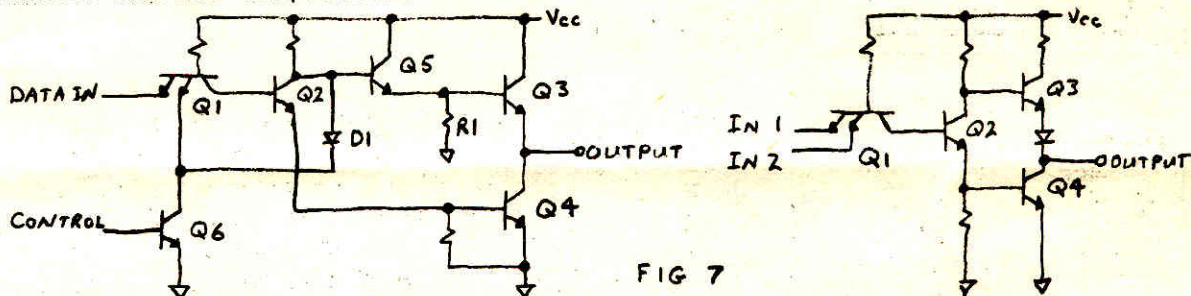


FIG 7

TYPICAL TSL GATE

TYPICAL TTL GATE

The actual operation of the gate as a tri-state device is made possible by the addition of Q5 (Darlington transistor for greater high level drive), Q6 (control input transistor), R1, and D1. The control input either enables the output or it disables it. When a high level is applied to the control input Q6 turns on and disables the input by pulling the emitter of Q1 low. D1 is now forward biased holding the base of Q5 low, which in turn holds Q3 off. Q4 is held off by the low level at the emitter of Q2. So, both Q3 and Q4 are turned off and the output is a floating high-impedance. This "looks like it has been disconnected from the bus and represents only a 40 microAmp. load (leakage current at both high and low levels). This is the hi-Z state. A very important factor is that the control input "floats" to a high level if no line is connected to it. Since this is an active low input, when the control is low the gate operates as a normal standard TTL gate.

This is a simplified explanation of how a TSL gate operates and in no way is intended to represent the actual detailed operation of "A" particular TSL integrated circuit. Any schematic representation of a TSL gate in a manufacturer's data book will differ from this "typical" gate.



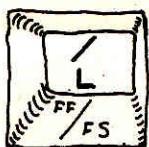
However, the operation is valid and described. The TSL design not only allows great bussing capabilities but also provides many side advantages including the speed of standard TTL, better noise immunity, higher drive capability, faster bus switching times, and some neat protective features.

The drive capability of a gate simply amounts to how much and how fast current can be moved, and all logic families are rated as to their sourcing and sinking capabilities. By this we determine how many inputs can be hung on an output, how much line or cable can be driven, and what you have to do to interface other logic families or types of circuits. TSL can source 5.2 milliAmp. at 2.4 Volts--13 times better than TTL--allowing up to 128 TSL collector-dots to drive 3 standard TTL inputs. TSL has at least 10 times the line driving capability of TTL. All this at standard TTL speeds.

The main protective advantage of TSL is that the outputs are self-protected from shorts to ground or overvoltage (to Vcc max). The output goes to its Hi-Z state with no input on the control, which is good and bad. Good, in that it may not interfere with some operations but bad in that it may be a bear to find in troubleshooting TSL lines.

The advancement of technology in the bus-system architecture has taken us from DTL wired-or to TTL open-collector to the TSL family which gives us all the advantages of non-bussed lines. This is not the end; but to date TSL is THE bussing logic.

#### HOBBYIST KEYBOARDS - Ken McGinnis



Most hobbyists know where to get some switches and almost any kind will work. Like everything else some are better than others. For most hobbyists the reed switch is probably the best (less expensive than Hal effect usually and less "bounce" or "jitter" than contact switches). Less "bounce" makes the wiring and circuitry simpler and more reliable.

The advantage of making your own is that you can work on it and change it any time you wish as well as self pride. No keyboard is EXACTLY like YOU want unless you design it.

Keytops are easy to change. Just buy a can of Krylon or Magic paint (Enamel takes longer to dry usually and may run easier). The directions say to use more than 1 coat. Most people try to finish quickly and end up spending more time by trying to cover with one coat. Then get some transfer lettering from the stationary store. One-character keys: 18-24 points

Two-character keys: 12-14 points

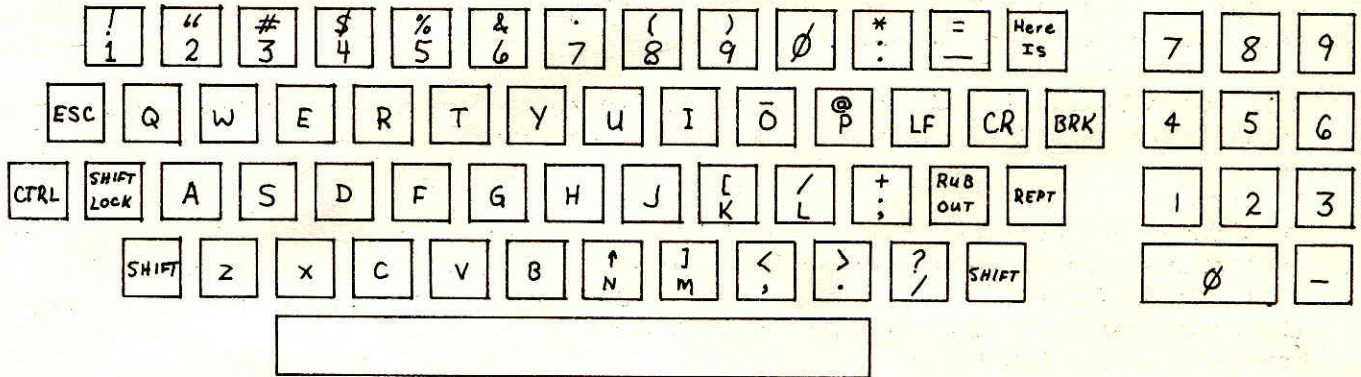
several characters or words: 8 points

These are easy to work with...Try it before you decide against it. Then spray with clear Krylon or Magic.

Encoding is easy with a ROM. Especially if you don't mind cutting, stripping and soldering a few wires. 2 ROMs are National: MM5740AAE (N-Key rollover) MM5740AAF (2-Key rollover). N-Key means the output is the same as the most recently depressed key even if the previous key hasn't been released yet. 2-Key means the output will not change until the key that produced that output is released.



This layout is from the National MOS book and is that of an ASR33. Paint some keys Red, yellow and blue with white characters and some keys White with black letters. You need 65 keys. I can get 65 microswitches (like new) in a cage for \$26.00.



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# HCC Glossary.....memories

Bipolar Semiconductors: "Old-style" semiconductor material, high-speed, medium-cost, medium in space and power required per circuit.

CMOS: Complimentary MOS; lower power but more expensive and lower packing density than ordinary MOS.

OEM: Original Equipment Manufacturer

PROM: Programmable ROM. A ROM in which the stored information can be altered, but not as easily as in a RAM. For example, in some PROM's, the contents may be erased by prolonged (minutes) application of ultra-violet light, and then re-written with relatively high power electronics. A core-memory version was called the EAROM (Electrically-Alterable ROM), and used multi-aperture cores.

RAM: Random-Access-Memory. Read and write from or to any memory location at high speed. There is no difference in the time required to operate to or from any address. Core memories are RAM's however the term is usually used with respect to semiconductor memories.

ROM: Read-Only-Memory. Information is permanently stored, and can be read from any location at high speed, but can never be altered.

SERIAL or DYNAMIC MEMORIES: Delay lines or their semiconductor equivalents, where stored information is inserted and propagates through the storage medium, and is only available for reading when it emerges at the other end; it must then be re-inserted, or it will be lost.

SOS: Silicon-On-Sapphire, a new technique which promises high speed, low power and high packing density.

VOLATILE and NON-VOLATILE MEMORIES: The stored information is lost if power is removed from a volatile memory.



DATA TRANSMISSION SYSTEM - Lee Felsenstein

Eric Dollard, 1360 Howard St., San Francisco, Ca. 94103, is working to put together a huge (10 kw) data transmission system, using surplus equipment from RCA's over-seas station at Point Reyes, California.

Eric needs help, since he has lots of transmitters, receivers, multiplexers, etc., donated (through Resource One, a non-profit corporation), but no place to put them.

He already has multiple independent sideband modulators feeding a 10 kw multi-band transmitter, power supply and multiple channel receivers. He is dreaming of a vast non-profit or amateur common-carrier data system, and needs help in formulating the idea, as well as wrestling the hardware.

RTTY/Computer enthusiasts should get in touch with Eric at the above address or leave a message at (415) 864-8063.

BULLETIN BOARD - Club Members

Your ALTAIR or similar size minicomputer in a CYBERCOM cabinet with intact card reader \$100.00. Steel cabinet for 12" monitor: 12" deep, 13" top, 14" bottom with plexiglass front: \$16 unfinished. Will quote aluminum (Anodized clear or black or unfinished) or finished steel to your specifications. Phi-Deck case with aluminum or steel face plate (15.00 single drive, \$22.00 for dual drive) Ken McGinnis, Box 2078, San Mateo, Ca. 94401

ALTAIR (system 1) in a CYBERCOM case with panel switches: rocker-type and rearranged in 2-3-3-2-3-3 fashion for easier octal entry. \$424.00 or trade for your unassembled ALTAIR. Ken McGinnis, Box 2078, San Mateo, Ca. 94401

ALTAIR compatible CPU boards \$12.00 if pre-pay, \$15.00 COD. Memories, 2102's, 500-600ns \$2.00 each. Please pre-pay. Send name, address, and home phone to: Robert Baer, 921 Lincoln Ave., Palo Alto, CA. Also available at club meetings.

MARK-8 1K word memory, TV typewriter, both working, \$350 or best offer. Keyboard free. John Neves 325-1873 Palo Alto, CA.

CLUB MEETINGS - 7PM

Meetings are held every two weeks at Stanford Linear Accelerator Center, Menlo Park, CA. Ask the guard for directions to the meeting location. Meeting dates are October 1st, 15th, 29th, etc. Meetings begin at 7PM and continue to 10 or 11PM.



# DATA FILE

00 000 001

MSH F	0	1	2	3	4	5	6	7
MSH B	F	E	D	C	B	A	9	8
LSH B								
—	—	16	32	48	64	80	96	112
F	1	17	33	49	65	81	97	113
E	2	18	34	50	66	82	98	114
D	3	19	35	51	67	83	99	115
C	4	20	36	52	68	84	100	116
B	5	21	37	53	69	85	101	117
A	6	22	38	54	70	86	102	118
9	7	23	39	55	71	87	103	119
8	8	24	40	56	72	88	104	120
7	9	25	41	57	73	89	105	121
6	10	26	42	58	74	90	106	122
5	11	27	43	59	75	91	107	123
4	12	28	44	60	76	92	108	124
3	13	29	45	61	77	93	109	125
2	14	30	46	62	78	94	110	126
1	15	31	47	63	79	95	111	127
0	16	32	48	64	80	96	112	—
LSH F								
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
A								
B								
C								
D								
E								
F								

MSH = Most significant Hex-Char.  
 LSH = Least "  
 F = Forward  
 B = Backward

Table to be used for M6800, M6801, M6802, and ECT  $\mu$ P branching instructions using  $\pm 127$  byte relative addressing.

Examples: BACK  $4_{10}$  BYTES = FC $_{16}$ , FORWARD  $42_{10}$  BYTES = 2A $_{16}$  BACK  $110_{10}$  BYTES = 92 $_{16}$

Find the number of bytes to branch inside the table; then read the Hex equivalent at top and side.

Contributed by: Ray Boaz, September 20, 1975

Robert Reiling, editor  
HOMEBREW COMPUTER CLUB NEWSLETTER  
Post Office Box 626  
Mountain View, CA 94040



FIRST CLASS MAIL

LENNY SHUSTEK  
P.O. BOX 3210  
STANFORD, CA.

94088